E1 Ultimate Limits of Integrated Electronics

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The time is right to search further for the ultimate limits of integrated electronics. The true limits, or whether they even exist, are debated and controversial given the industry's continued accelerated technological progress. Regardless of whether a definitive conclusion can be drawn, even a bit of understanding is vital, as progress in the right direction will impact the entire industry's efforts to sustain its revenue and profit growth at the soaring rates seen since the 1960s. Current research results show a functional FET device with the gate length below 10 nm and that future CMOS technology can be manufactured at 25 nm feature sizes, a level hardly projected by many of the preeminent commentators in the last few decades. Governing physics seems more forgiving than expected, as technologists and designers continually make breakthroughs. The questions of how to scale below the 25 nm and what the laws of nature really allow need to be answered.

Keyes (IEEE Spectrum 1969, Proc. 1975, T-ED 1979), Mead (SSE 1972), Dennard (JSSC 1974), Meindl (ISSCC 1975, 1981, 1992), Moore (IEDM 1975, ISSCC 2003), and many other experts in our technical societies have explored these limits. But the current technology scaling from a 130 nm toward a 32 nm technology node has been progressing much faster than expected as driven by NAND flash memories (Hwang, ISSCC 2002) and super-logic-chips. Such a complicated subject should stimulate our panelists and the ISSCC attendees to think about research, manufacturing, and business impacts by using Meindl's hierarchical study methodologies: (a) Fundamental limits: how small of device dimensions and how large of chip capacities will be limited by thermodynamics requiring energy per binary digital switching or overcoming various noises? Will multilevel signals stored in memories or switched by non-binary logic be able to extend these limits? (b) Material limits: what is the ultimate transit time of an electron in present scaled integrated-silicon-material-system and how can this limit be surpassed by the nano-engineering of other semiconductor system, such as SiGe, strained Ge, Hf-based silicates, etc.? (c) Device limits: Can statistical variations be effectively controlled into deep-nanometer technology regimes? Will SOI really help? Will another structural innovation transform the current paradigm of evolutionary device scaling?(d) Circuit limits: Can the CMOS-switching system still serve as an effective platform for controllable power dissipation? Will today's die-to-package system soon reach a speed or power limit due to the inelegant interconnection system expanded via conventional ways? (e) System limits: what is the optimized architecture: SOC versus SIP, homogeneous versus heterogeneous integration (Lu, ISSCC 2004), programmable versus application specific, software versus hardware solutions, etc.? How can the "Heat Removal" limits of system chips we have experienced so far be further improved, or to what degree?

This panel will be moderated by asking each panelist to comment on following specific questions followed by immediate interactions with audiences: (1) The limit of scaling is application dependent; state the application in your interest and at which technology node will CMOS-scaling stop working for this application? Which design - logic, memory, or analog - will face the limit first? (2) What are the most difficult obstacles based on device physics? (3) How will circuit design change in the face of limitations at the device level? (4) How can system architecture extend the life of CMOS, such as hardware/software co-design, programmable systems, and parallel processing? (5) Will 3D, chip stack, or multi-dimensional die-integration system chips (SC) help continue technological progress from IC toward super-function SC? (6) Will new material systems such as Ge, III-V, carbon nanotubes, or semiconductor nano-wires help extend the CMOS life? Or are there fundamental limitations dictated by the laws of physics that cannot be surmounted, irrespective of the materials? (7) What applications (new or existing) will be the economic drivers for the IC industry? What are the business model and the industrial/academic infrastructure most suitable for these applications to enable sufficient profit return on huge investments?

Should we expect a 2.5 nm technology? Shall we see an entire one of nowadays' supercomputers integrated into a single packaged SC with all xC functions (an anticipated terminology extending from today's 5C - Computer, Communication, Consumer, Control, Car)? This panel discussion will lead IC industry experts to investigate the limits of our current evolutionary approach and those set by the laws of physics; to assess further whether or how our IC industry can survive under a single-digit annual compound growth rate with sufficient profit margins; and to explore what new routes can the integrated electronics industry take to the ultimate boundaries of nature.

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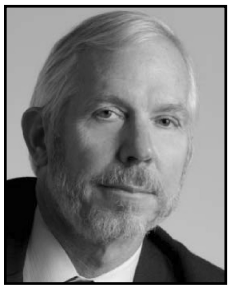
Mark Bohr, Intel, Hillsboro, OR
Moore's Law describing the benefits of increasing transistor count combined with Dennard's scaling theory describing the performance and power benefits of scaled transistors have been powerful drivers behind the rapid growth of the integrated circuits industry over the past 40 years. But how long will this continue? The demise of both Moore's Law and MOSFET scaling has often been predicted, only to be given new life by the inventiveness of our industry. For high performance logic products, there are several potential candidates for being ultimate limiters, including the fundamental scalability of MOSFETs, interconnect delay, variability, power, and cost. It is almost impossible to predict which of these will be the limiter, but the combination of these factors will ultimately lead to the limit of electron charge based device scaling. But as in the past, innovation will extend that time beyond what we can see today and novel technologies will likely emerge to push scaling even further.

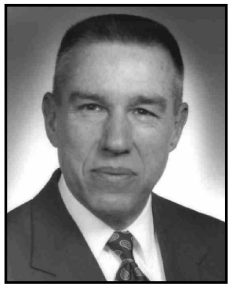


Robert Brodersen, University of California Berkeley, Berkeley, CA
I distrust predictions of a new ultimate limit to CMOS, since I have heard that many times in the past. However, this doesn't mean that the circuits and architectures that we have used will continue to be relevant, since I do believe future CMOS devices will have characteristics very different from what we have now. Already, we are having a fundamental shift in our processor architectures to parallel structures which can exploit density increases to increase performance rather than just device speed. Power density limitations and increased device variability will continue to cause us to evolve our circuits and architectures in even more dramatic ways. The key to keep scaling on track will be for the device developers to work with circuit and system designers to develop technologies we can actually use and for the designers to relax device requirements (e.g. device speed) that can be overcome with new system architectures.

Kiyoo Itoh, Hitachi, Tokyo, Japan
The power supply voltages of high-speed nanoscale CMOS LSIs continue to rise with device scaling, causing ever more serious power crises. This is mainly due to leakage and variability problems. Unfortunately, however, it seems to me that technologies to tackle the problems have not yet been developed sufficiently or consistently even for the 32-nm technology generation. Thus, key technologies such as dynamic CMOS circuits to eliminate a Vt drop yet keep leakage low and new MOSFETs with reduced Vt variations (e.g., low-cost FD-SOIs) must be developed before the ultimate limits of the technology can be foreseen. In addition, using planar-capacitor DRAM cells instead of existing SRAM cells for low-cost low-voltage LSIs might be necessary because they could resolve the large cell and narrow voltage margin problems inherent in SRAM cells.

Won-Sung Lee, Samsung, Giheung-Gu Yongin-City, Gyeonggi-Do, Korea
For the past few years, NAND flash bit-density growth rate has been larger than any other semiconductor devices, and expected to reach 50nm regime first at commercial production stage. Not only by aggressive physical scaling, the growth rate has been accelerated further by implementing multi (at present two)-bit per cell technology.

This talk will go over a variety of issues related to increasing the NAND flash bit density for data storage applications; the physical limits of scaling and non-scalable factors for NAND flash operation, the trade-off between device performance and reliability, error correction schemes to put more states in a given threshold voltage window, adoption of high-k dielectrics to reduce electric field interference during operations. This talk will also summarize the challenges and the future of NAND flash for data storage device in the mobile era.



J. D. Meindl, Georgia Institute of Technology, Altanta, GA
Early 21st century microchips are a marvelous consequence of a "fusion of the top-down and bottom-up approaches to nanotechnololgy." Top-down nanotechnology has been used to pattern and produce multibillion transistor chips with minimum feature sizes now approaching 50 nm. Bottom-up nanotechnology has been used to produce self-assembled single crystal ingots of silicon that are sliced to provide 300 mm diameter wafers for microchip manufacturing. Given the foregoing observation, what can be said about the future prospect of microchips continuing as the most powerful driver of the information revolution during the next half-century? One broad prospective is that to continue to advance silicon microchip technology toward its ultimate limits and eventually to replace it will entail an elegant "fusion of top-down and bottom-up nanotechnology enabled by discoveries and inventions in both physical and biological science and engineering" as profound as the mid-20th century inventions of the transistor and the integrated circuit.

Hans Stork, Texas Instruments, Dallas, TX
Physics tells us that CMOS gate scaling can continue for another order of magnitude beyond today. This means the industry should count on its historical 70% shrink until the end of the next decade. However, achieving this scaling will require overcoming a number of major challenges.

Business economics will continue to be the driving factor of our industry, and high density and low power logic applications will justify the largest investments. For those applications, the economics of patterning, the variability of electrical parameters and the efficiency of designing complex systems drive R&D.The search is still on for a cost effective successor to optical lithography, which is once again expected to run out in two generations. Huge numbers of small features result in inherently large variations. These will require radical changes in circuit and system design, as well as an order of magnitude improvement in EDA productivity to keep up with changes in the market.